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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/225,388	01/05/1999	DAVID W SMITH	2000.002500	2528
23720	7590	01/26/2005	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			NGUYEN, TOAN D	
			ART UNIT	PAPER NUMBER
			2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/225,388	<b>Applicant(s)</b> SMITH, DAVID W	
	<b>Examiner</b> Toan D Nguy n	<b>Art Unit</b> 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 August 2004.  
 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-35 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-6, 8-18, 20-28 and 30-35 is/are rejected.  
 7) ☒ Claim(s) 7, 19 and 29 is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 21 November 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \* c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2, 9, 23-24, 31-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaughan et al. (US 5,802,305) in view of Goffinet et al. (US 5,905,906).

For claim 1, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a set of data signals from an external data source (figure 4, col. 8 lines 45-47);

decoding said received set of data signals (col. 8 lines 47-50);

extracting a destination address from said set of data signals (col. 8 lines 47-50);  
comparing said destination address extracted from said data signals to a known data value (col. 8 lines 52-54);

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value (col. 8 lines 54-58); generating at least one status

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signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry (col. 8 lines 59-64); and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (figure 4, col. 8 lines 59-64).

However, McKaughan et al. does not disclose detecting a size of said received set of data signals. In an analogous art, Goffnet et al. disclose detecting a size of said received set of data signals (col. 16 lines 17-19).

One skilled in the art would have recognized detecting a size of said received set of data signals to use the teachings of Goffnet et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the detecting a size of said received set of data signals as taught by Goffnet et al. in McKaughan et al.'s system with the motivation being determine if the packet is of the correct length and the number of bytes (col. 16 lines 15-16).

For claims 2 and 24, McKaughan et al. disclose set of data signal received is data packet that is in a serial data format, over a network line (col. 8 lines 45-47).

For claims 9 and 31, McKaughan et al. disclose wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host that a address match has been found (figure 4, col. 59-62).

For claim 23, the claim is directed to the same subject matter as in claim 1. Therefore, it is subject to the same rejection.

For claim 32, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a data signal (figure 4, col. 8 lines 45-47);

extracting a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; (col. 8 lines 47-54);and

waking up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed (figure 4, col. 8 lines 59-64).

For claim 34, the claim is directed to the same subject matter as in claim 32. Therefore, it is subject to the same rejection.

3. Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaughan et al. (US 5,802,305) in view of Goffinet et al. (US 5,905,906) and Warren et al. (US 4,516,201) further in view of Pai (US 4,130,874).

For claims 3-6, 8, 25-28, 30 and 33, McKaughan et al. do not disclose step of detecting a size of said received set of data signal and decoding said received set of data signals, includes:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a member held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;  
using said word count to address data stored in a memory circuitry; and  
inputting a set of data signals from said memory circuitry into an appropriate  
comparator. In an analogous art, Warren et al. disclose:

converting said serial data packet into a parallel data format (figure 2, col. 8 lines  
23-28);

extracting a word clock from said received data packet (figure 5, col. 14 lines 14-  
16);

incrementing a member held by said counter, said word clock generating a word  
count (figure 6, col. 16 lines 1-52);

inputting said converted parallel format data into a plurality of comparators (figure  
8, col. 23 lines 38-68);

using said word count to address data stored in a memory circuitry (col. 23 lines  
3-5); and

inputting a set of data signals from said memory circuitry into an appropriate  
comparator (figure 8, col. 23 lines 38-68);

Warren et al. disclose further wherein said act of extracting a destination address  
from said set of data signals further comprises slicing said parallel data such that at  
least one destination address data word is generated (col. 8 lines 23-28 as set forth in  
claims 4 and 26); performing a comparison function upon said converted, parallel set of  
data signals, and said set of data from said memory circuitry (figure 8, col. 23 lines 38-  
68), generating a digital comparator status signal in response of said performance of

comparator function; and clocking in said digital comparator data signal into a register (figure 8, col. 23 line 27-68 as set forth in claims 5 and 27); determining whether said received data signals should be received by a host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry (figure 2, col. 8 lines 23-28 as set forth in claims 6 and 28); performing an OR function upon all said latched output of said comparator (figure 7, col. 21 lines 33-38 as set forth in claims 8 and 30).

One skilled in the art would have recognized converting said serial data packet into a parallel data format to use the teachings of Warren et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use the converter as taught by Warren et al: in McKaughan et al.'s system with the motivation being to turn its serial input into selectably 5-bit or 8-bit parallel words (col. 8 lines 25-26).

However, McKaughan et al. in view of Warren et al. do not disclose a plurality of comparators. In an analogous art, Pai discloses a plurality of comparators (figure 2, col. 6 lines 29-31).

One skilled in the art would have recognized a plurality of comparators to use the teachings of Pai in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the plurality of comparators as taught by Pai in McKaughan et al.'s system with the motivation being to produce an equally logic signal at the outputs 50, 51 and 52 of the comparator circuits 42, 43 and 44, respectively (col. 6 lines 45-47).

For claims 10-18, 20-22 and 35, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card, comprising:

means for receiving a data signal (figure 4, col. 8 lines 45-47);

a counter (col. 6 line 43);

a host circuitry interface capable of transmitting and receiving data from a host circuitry said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry, said decoded address data being extracted from said data signal (figure 1, col. 6 lines 26-29);

a memory circuitry (figure 2, col. 6 line 42-03);

a mask circuitry (col. 8 line 48).

McKaughan et al. does not disclose means for detecting a size of said received set of data signals- In an analogous art, Goffinet et al. disclose means for detecting a size of said received set of data signals (col. 16 lines 17-19).

One skilled in the art would have recognized means for detecting a size of said received set of data signals to use the teachings of Goffinet et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the means for detecting a size of said received set of data signals as taught by Goffinet et al. in McKaughan et al.'s system with the motivation being determine if the packet is of the correct length and the number of bytes (col. 16 lines 15-16).

However, McKaughan et al. in view of Goffinet et al. do not disclose:



a data formatter;

a clock divider;

a plurality of comparators;

a digital logic circuitry;

a plurality of status registers and a plurality of clocked registers. In an analogous art, Warren et al. disclose:

a data formatter (figure 1, col. 6 lines 37-02);

a clock divider (col. 30 line 49);

a digital logic circuitry (figure 2, col. 8 lines 23-28);

a plurality of status registers and a plurality of clocked registers (figure 10, col. 30 lines 18-64).

Warren et al. disclose further formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream (figure 2, col. 8 lines 10-37 as set forth in claim 11); memory circuitry comprises of a memory element and a memory data access logic (figure 7, col. 12 lines 20-29 as set forth in claims 13 and 14); memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements (figure 2, col. 8 lines 3-24 as set forth in claims 15 and 22); and comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter (figure 8, col. 23 lines 38-68 as set forth in claims 16-18 and 20-21).

One skilled in the art would have recognized a data formatter to use the teachings of Warren et al. in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use the data formatter as taught by Warren et al. in McKaughan et al.'s system with the motivation being to provide the host with status information concerning the data link, to inform the host, to take action when predetermined characters are received, to automatically generate the protocol characters required when transmitting and eliminate such characters when receiving (col. 6 lines 43-48).

McKaughan et al. in view of Goffinet et al. and Warren et al. do not disclose a plurality of comparators. In an analogous art, Pai discloses a plurality of comparators (figure 2, col. 6 lines 29-31).

One skilled in the art would have recognized a plurality of comparators to use the teachings of Pai in the system of McKaughan et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the plurality of comparators as taught by Pai in McKaughan et al.'s system with the motivation being to produce an equally logic signal at the outputs 50, 51 and 52 of the comparator circuits 42, 43 and 44, respectively (col. 6 lines 45-47).

#### ***Allowable Subject Matter***

4. Claims 7, 19 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Arguments***

5. Applicant's arguments filed August 16, 2004 have been fully considered but they are not persuasive.

The applicant argues with respect to claims 1, 10, 23, 32 and 34, that the mere disclosure of data size checking by Goffinet would not lead one of ordinary skill in the art having benefit of McKaughlin would not make obvious the element of detecting a size of the received set of data signals of the claims. The examiner disagrees. Applicant's attention is directed to Goffinet patent at col. 2 lines 30-52, where Goffinet clearly teaches "that the size (in bytes) of the response message from the printer depends upon which specific variable of the configuration information has been queried by the host computer." Goffinet clearly teaches a computer in a computer network that detecting a size of said received set of data signals (figure 1). The primary reference, McKaughlin teaches "In a computer network including a plurality of interconnected computers" (Abstract lines 1-2). Therefore, Goffinet, secondary reference) is used to incorporate the primary reference, McKaughlin.

Furthermore, applicant argues that McKaughan does not detecting the size of the received set of signals when determining whether to wake up the computer, which is an element called for by the claims. The examiner disagrees. McKaughan refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card of sleeping computers detects an incoming packet and compares the incoming packet to a list of packets stored on the network interface cards. McKaughan then compares the received packet to a list of packets on the card and provides a wake-up sequence of a remote computer (col. 6 lines 43-64). By comparing

the received packet to a list of packets on the card, McKaughan detecting length (size) of packet (col. 8 line 1).

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

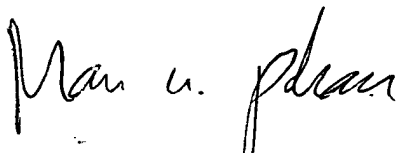
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MAN U. PHAN  
PRIMARY EXAMINER